CLAIMS

1. A method for integrating copper with an MIM capacitor during the formation said MIM capacitor, said method comprising the steps of:

forming an MIM capacitor upon a substrate; and

depositing at least one copper layer upon said substrate and layers thereof to form at least one metal layer from which said MIM capacitor is formed, such that said MIM capacitor may be adapted for use with an embedded DRAM device.

2. The method of claim 1 wherein said MIM capacitor comprises a low-temperature MIM capacitor.

3. The method of claim 1 further comprising the step of:

forming at least one DRAM crown photo layer upon said substrate and layers thereof to form said MIM capacitor.

4. The method of claim 1 further comprising the steps of:

forming transistors upon said substrate and layers thereof during a FEOL manufacturing operation;

thereafter forming an interlayer dielectric (ILD) layer upon said substrate and layers thereof;

thereafter forming at least one contact upon said substrate and layers thereof; and

then forming at least one W-plug formation upon said substrate and layers thereof.

5. The method of claim 4 further comprising the steps of:

depositing a metal-1 oxide layer upon said substrate and layers thereof through a SiN/FSG/SiN deposition operation;

performing a photo and etch patterning operation upon said substrate and layers thereof;

depositing a layer comprising Ta/Cu upon said substrate and layers thereof; and

performing a copper CMP operation upon said substrate and layers thereof.

6. The method of claim 5 further comprising the steps of:

depositing a metal-2 oxide-1 layer upon said substrate and layers thereof through a SiN/FSG/SiN deposition operation;

thereafter performing a DRAM node photo and etch operation upon said substrate and layers thereof.

7. The method of claim 6 further comprising the steps of:

performing a TaN sputter operation upon said substrate and layers thereof;

thereafter performing a photoresist coating and etch operation upon said substrate and layers thereof to form at least one recess in a DRAM cell node; and

then performing a photoresist strip operation upon said substrate and layers thereof.

8. The method of claim 7 wherein the step of thereafter performing a photoresist coating and etch operation upon said substrate and layers thereof to form at least one recess in a DRAM cell node, further comprises the step of:

thereafter performing a BARC coating and etch operation upon said substrate and layers thereof to form at least one recess in a DRAM cell node.

9. The method of claim 7 further comprising the steps of:

performing a Ta_2O_5/TaN/Cu deposition operation upon said substrate and layers thereof;

thereafter performing a copper CMP operation upon said substrate and layers thereof; and

performing an SiN removal operation upon said substrate and layers thereof.

10. The method of claim 9 further comprising the steps of:

depositing a metal-2 oxide 2 layer through SiN/FSG/SiON deposition upon said substrate and layers thereof;

thereafter performing a VIA-1 photo and etch operation upon said substrate and layers thereof.

11. The method of claim 10 further comprising the steps of:

performing a metal-2 I-line BARC coating operation upon said substrate and layers thereof; and

thereafter performing an etch back operation upon said substrate and layers thereof.

12. The method of claim 11 further comprising the steps of:

performing a metal-2 oxide photo and etch operation upon said substrate and layers thereof to define at least one logic metal-2 layer and a DRAM top plate; and

thereafter removing a stop layer thereof.

13. The method of claim 12 further comprising the steps of:

performing a TaN/Cu deposition operation; and

thereafter performing a copper CMP operation upon said substrate and layers thereof.

14. The method of claim 13 further comprising the steps of:

thereafter performing standard BEOL semiconductor fabrication operations to form said MIM capacitor upon said substrate.

15. The method of claim 14 further comprising step of:

varying a sequential formation said at least one DRAM crown photo layer upon said substrate and layers thereof in order to improve an associated capacitance of said MIM capacitor.

16. The method of claim 1 further comprising the step of:

forming said MIM capacitor utilizing at least one black diamond layer, wherein said at least one black diamond layer possesses a low K value, thereby permitting an associated AC delay to be decreased, while increased associated speeds thereof.

17. The method of claim 16 further comprising the steps of:

forming said at least one black diamond layer above an SiC layer; and

forming a SiON layer above said at least one black diamond layer.

18. An MIM capacitor which integrates copper deposition during the formation of said MIM capacitor, said MIM capacitor comprising:

an MIM capacitor formed upon a substrate; and

at least one copper layer deposited upon said substrate and layers thereof to form at least one metal layer from which said MIM capacitor is formed, such that said MIM capacitor may be adapted for use with an embedded DRAM device.

19. The MIM capacitor of claim 18 wherein said MIM capacitor comprises a low-temperature MIM capacitor.

20. The MIM capacitor of claim 18 wherein at least one DRAM crown photo layer is formed upon said substrate and layers thereof to form said MIM capacitor.

21. The MIM capacitor of claim 18 further comprising:

at least one transistor formed upon said substrate and layers thereof during a FEOL manufacturing operation;

an interlayer dielectric (ILD) layer formed upon said substrate and layers thereof;

at least one contact formed upon said substrate and layers thereof; and

at least one W-plug formation formed upon said substrate and layers thereof.

22. The MIM capacitor of claim 21 further comprising:

a metal-1 oxide layer deposited upon said substrate and layers thereof through a SiN/FSG/SiN deposition operation, wherein a photo and etch patterning operation is thereafter upon said substrate and layers thereof; and

a layer comprising Ta/Cu formed upon said substrate and layers thereof, wherein a copper CMP operation is subsequently upon said substrate and layers thereof.

23. The MIM capacitor of claim 22 further comprising:

a metal-2 oxide-1 layer deposited upon said substrate and layers thereof through a SiN/FSG/SiN deposition operation, wherein a DRAM node photo and etch operation is thereafter performed upon said substrate and layers thereof.

24. The MIM capacitor of claim 23 wherein said substrate and layers thereof are subject to a TaN sputter operation followed by a photoresist coating and etch operation to form at least one recess in a DRAM cell node; and

wherein a photoresist strip operation is thereafter performed upon said substrate and layers thereof.

25. The MIM capacitor of claim 24 wherein a BARC coating and etch operation is performed upon said substrate and layers thereof to form at least one recess in a DRAM cell node.

26. The MIM capacitor of claim 24 wherein said substrate and layers are subject to Ta_2O_5/TaN/Cu deposition operation followed by the performance of a copper CMP operation and an SiN removal operation upon said substrate and layers thereof.

27. The MIM capacitor of claim 26 further comprising:

a metal-2 oxide 2 layer deposited through SiN/FSG/SiON deposition upon said substrate and layers thereof, wherein a VIA-1 photo and etch operation is thereafter upon said substrate and layers thereof.

28. The MIM capacitor of claim 27 wherein said substrate and layers thereof are subject to a metal-2 I-line BARC coating operation and thereafter to an etch back operation.

29. The MIM capacitor of claim 28 wherein said substrate and layers thereof are subject to a metal-2 oxide photo and etch operation to define at least one logic metal-2 layer and a DRAM top plate, such that stop layer thereof is thereafter removed.

30. The MIM capacitor of claim 29 wherein said substrate and layers thereof are subject to a TaN/Cu deposition operation and a performance of a copper CMP operation.

31. The MIM capacitor of claim 30 wherein said substrate and layers thereof are subject to the performance of standard BEOL semiconductor fabrication operations to form said MIM capacitor upon said substrate.

32. The MIM capacitor of claim 31 wherein sequential formation of said at least one DRAM crown photo layer upon said substrate and layers thereof can be varied in order to improve an associated capacitance of said MIM capacitor.

33. The MIM capacitor of claim 18 further comprising:

at least one black diamond layer, wherein said at least one black diamond layer possesses a low K value, thereby permitting an associated AC delay to be decreased, while increased associated speeds thereof.

34. The MIM capacitor of claim 33 further comprising:

said at least one black diamond layer located above an SiC layer; and

A SiON layer located above said at least one black diamond layer.